In the Claims:

1-21 (Cancelled)

22. (New) Circuitry for receiving a time varying input signal and for generating an oscillating output signal and a mixed output signal, comprising:

a differential transistor pair for receiving the time varying input signal and for generating a differential pair output signal having a time varying input signal component and other signal components;

a first filter network, coupled to the differential pair at a pair of nodes, for receiving the time varying input signal component and for selectively providing the oscillating output signal through a negative resistance generated between the pair of nodes; and

a second filter network, coupled to the pair of nodes, for receiving the oscillating output signal, and also coupled to the differential pair for receiving the other signal components and for generating and selectively passing the mixed output signal.

23. (New) The circuitry of claim 22, wherein the time varying input signal has time varying and constant components.

24. (New) The circuitry of claim 22, wherein the magnitude of the negative resistance is proportional to the magnitude and frequency of the time varying input signal.

25. (New) The circuitry of claim 22, wherein the first filter network generates the negative resistance across nodes connected to the collectors of the differential pair of transistors.

26. (New) The circuitry of claim 22, wherein the second filter network includes means for generating the mixed output signal by translation of the oscillating output signal by the frequency of the time varying signal.

27. (New) The circuitry of claim 26, wherein the mixed output signal has a frequency equal to the frequency of the oscillating output signal plus the frequency of the time varying input signal.

28. (New) The circuitry of claim 26, wherein the mixed output signal has a frequency equal to the frequency of the oscillating output signal minus the frequency of the time varying input signal.

29. (New) The circuitry of claim 22, further comprising:

a second differential transistor pair for receiving a second time varying input signal, the second differential transistor pair being coupled to the first and second filter networks for providing the second time varying input signal;

wherein the first filter network creates a negative resistance across two pairs of nodes in parallel with each other, and wherein the second filter network cancels output signals at the frequency of the oscillating output signal.

30. (New) The circuitry of claim 29, wherein the first and second time varying signals have time varying and constant components.

31. (New) The circuitry of claim 29, wherein the first and second time varying signals are out of phase with each other.

32. (New) The circuitry of claim 29, wherein the overall negative resistance of the parallel negative resistances is substantially constant.

33. (New) The circuitry of claim 22, wherein the first filter network is a high pass filter.

34. (New) The circuitry of claim 33, wherein the high pass filter is tuneable.

35. (New) The circuitry of claim 22, wherein the second filter network is a low pass filter.

36. (New) The circuitry of claim 22 wherein the first filter network is a low pass filter.

37. (New) The circuitry of claim 36, wherein the low pass filter is tuneable.

38. (New) Apparatus, comprising:

means for receiving a time varying input signal and for generating an output signal having a time varying input signal component and other signal components;

means, coupled to the means for receiving a time varying input signal at a pair of nodes, for receiving the time varying input signal component and for selectively providing an oscillating output signal through a negative resistance generated between the pair of nodes; and

means, coupled to the pair of nodes, for receiving the oscillating output signal, and also coupled to the means for receiving a time varying input signal, for receiving the other signal components and for generating and selectively passing a mixed output signal.

39. (New) A mixillator circuit, comprising:

a pair of transistors each having a first, a second and a third terminal, wherein the first terminals of the pair of transistors are coupled together and connected to a time varying input signal;

a first filter network coupled to the second and third terminals of the pair of transistors, for receiving the time varying input signal and for generating an oscillator output signal; and

a second filter network, coupled to the third terminals of the pair of transistors, for receiving the oscillator output signal and for generating a mixer output signal by translating the oscillator output signal.

40. (New) The mixillator circuit of claim 39, wherein the pair of transistors are bipolar junction transistors, and wherein the first, second and third terminals of the pair of transistors are respectively the emitter, base and collector terminals of the bipolar junction transistors.

41. (New) The mixillator circuit of claim 39, wherein the first filter network provides a negative resistance between the third terminals of the pair of transistors.

42. (New) The mixillator circuit of claim 39, further comprising a current source coupled to the first terminals of the pair of transistors for providing the time varying input signal.

43. (New) The mixillator circuit of claim 42, wherein the time varying input signal includes DC current components and time varying current components.

44. (New) The mixillator circuit of claim 41, wherein the first filter network provides a negative resistance at a desired oscillator frequency, Fosc.

45. (New) The mixillator circuit of claim 44, wherein the first filter network does not provide a negative resistance at a desired mixer frequency, Fmixer, wherein Fmixer is at a distinct frequency from Fosc.

46. (New) The mixillator circuit of claim 39, wherein the second filter network blocks the oscillator output signal.

47. (New) The mixillator circuit of claim 39, wherein the second filter network generates the mixer output signal by translating the oscillator output signal by a positive amount equal to the frequency of the time varying input signal.

48. (New) The mixillator circuit of claim 39, wherein the second filter network generates the mixer output signal by translating the oscillator output signal by a negative amount equal to the frequency of the time varying input signal.